High Performance, High Yield Millimeter-Wave MMIC LNAs Using InP HEMTs

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ABSTRACT

A millimeter-wave MMIC low noise amplifier chip set has been developed. Based on the InP HEMT technology, these LNAs provide state-of-the-art performance as well as excellent yield and repeatability. With greater than 50% chip yield, a three-stage Q-band LNA design achieved 26 to 31 dB of gain from 42 to 50 GHz and 1.8 dB average noise figure from 43.3 to 45.7 GHz. In addition, there are six other LNA designs including a four-stage V-band LNA with 28 dB of gain and 2.3 dB noise figure and a two-stage balanced Q-band LNA that provided 17 dB of gain and has greater than 61% yield.

INTRODUCTION

The pursuit of improved communication satellite systems has created a need for monolithic microwave integrated circuits (MMIC). There are good reasons for their popularity. MMICs can reduce the size and weight significantly as well as enhance the reliability of any payload. In addition to these advantages, MMICs can also provide outstanding electrical performance with excellent repeatability and yield. Our previous MMIC LNA results were presented at last year's symposium and show-cased state-of-the-art noise figure performance [1]. As a continuation of that effort, this MMIC chip set shows significant improvements in RF performance in addition to achieving excellent yield for Q-band and V-band MMIC LNAs using the InP HEMT technology developed at Hughes Research Laboratory. In this paper, we discuss the HEMT structure, the design software and models, followed by descriptions of the designs and test results.

InP HEMT STRUCTURE

Lattice-matched to a 3 inch InP semi-insulating substrate, the InP HEMT structure consists of a 250 nm undoped AlInAs buffer with a 40 nm GaInAs channel, a 1.5 nm undoped spacer, an 8 nm AlInAs donor layer, and a 7 nm GaInAs doped cap. The electron sheet density is around 2.7×10^{12} cm^{-2} and the electron mobility is between 10,000 to 11,000 cm^2/Vs at 25°C. A double-exposure e-beam lithography process is used to create a highly repeatable 0.1 μm gate definition through the resist. To shield the active device from moisture and contamination, a 100 nm thick silicon nitride passivation layer is used [2].

DESIGN SOFTWARE AND MODELING

All circuit-level simulations and layouts were done using HP-EEsof's Academy/Libra™ software. Microstrip discontinuities, such as tee-junctions and cross-junctions, were analyzed using Sonnet em™. A 17-element HEMT model developed from measured data was used to generate the s-parameters at Q-band and V-band. The noise model was generated from discrete devices that were characterized for noise figure.

MMIC DESIGNS AND TEST RESULTS

THREE-STAGE Q-BAND LNA

Residing inside a 1.5 × 3.0 mm chip periphery, this circuit uses three 50 × 0.1 μm InP HEMTs (see Figure 1). The first two stages are biased and matched for low-noise (1V at 7.5 mA); the last stage is biased and matched for high gain (1.5V at 10 mA). MIM capacitors and microstrip lines are used for the matching circuits. Quarter-wave line, radial stubs and epi resistors are used as part of the stabilizing circuits. Total dc power dissipation of this chip is 30 mW which translates into a figure-of-merit of 1.2 mW/dB. All sites on the wafer were tested using the Cascade Microtech probe station and the HP8510C Network Analyzer. A yield of 51% was achieved using a

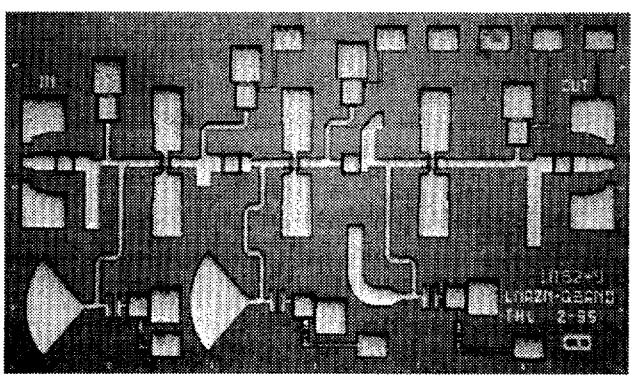

Figure 1. Layout of three-stage Q-band MMIC LNA

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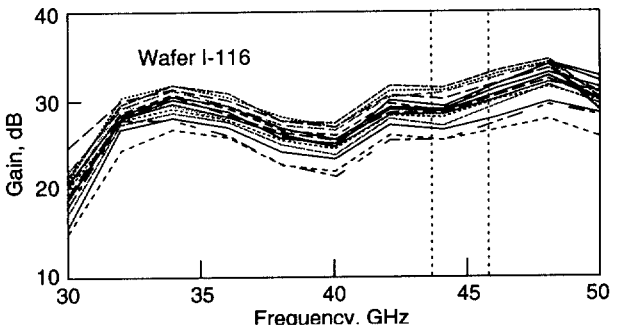

Figure 2a. Yield data for three-stage Q-band MMIC LNA

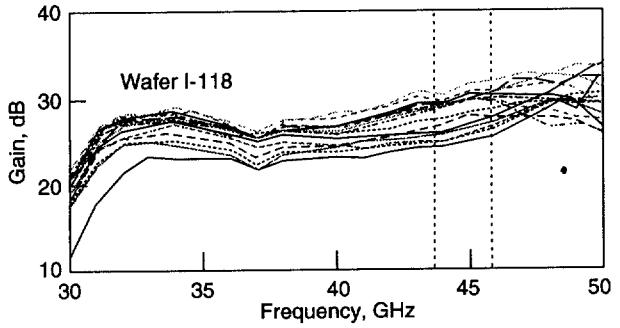

Figure 2b. Yield data for three-stage Q-band MMIC LNA

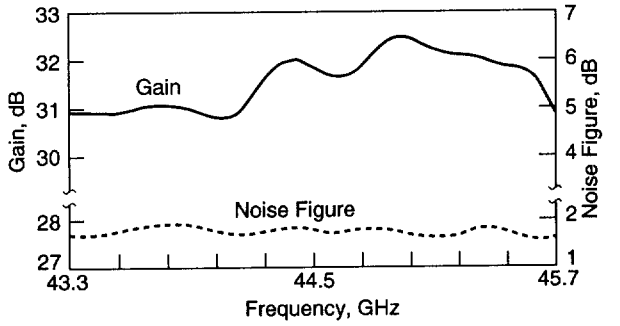

Figure 2c. Gain and noise figure for three-stage Q-band MMIC LNA

gain specification of 25 dB minimum from 42 to 50 GHz (see Figure 2a and 2b). The average noise figure, de-embedded to the MMIC, measured in a test fixture is 1.8 dB from 43.3 to 45.7 GHz and to our knowledge, is the best average noise figure for a three-stage MMIC LNA in this frequency band (see Figure 2c).

FOUR-STAGE Q-BAND LNA

The high gain and low noise performance of this MMIC is based on four 50 × 0.1 μm HEMTs (see Figure 3). Input, output and interstage matching are done in a similar manner as the previous three-stage LNA. The first two stages are matched and biased for low noise (1V at 7.5 mA) while the third and fourth stage are matched and biased for high gain (1.5V at 10 mA). Every site of this four-stage LNA on the wafer, which had fewer repeats in the reticle than the 3-stage LNA, was tested for small-signal gain. The test results show that 56% of the chips

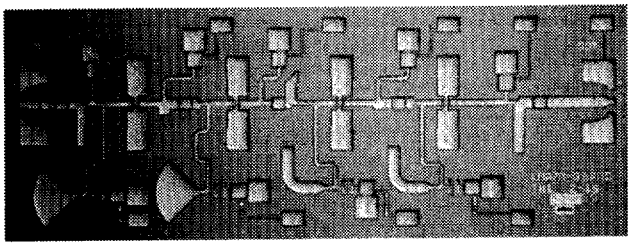

Figure 3. Layout of four-stage Q-band MMIC LNA

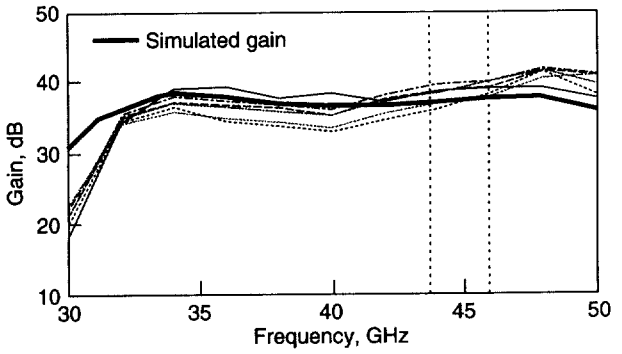

Figure 4. Yield data for four-stage Q-band MMIC LNA

have greater than 35 dB of gain from 42 to 50 GHz (see Figure 4). Noise figure will be measured in a test fixture and we expect the result to be less than 2.0 dB from 43.5 to 46.5 GHz. This MMIC is 1.5 × 4.0 mm in size and consumes 45 mW of dc power for a figure-of-merit of 1.3 mW/dB.

TWO-STAGE Q-BAND LNA

Like the previous two designs, 50 × 0.1 μm devices were used in this design to minimize dc power consumption (see Figure 5). Both devices are biased and matched at the low noise condition (1V at 7.5 mA). The MMIC chip dissipates only 15 mW of dc power resulting in only 0.9 mW/dB. 46% of these LNAs provided better than 16 dB of gain from 42 to 50 GHz (see Figure 6a). An average noise figure of 1.8 dB was measured from 43.3

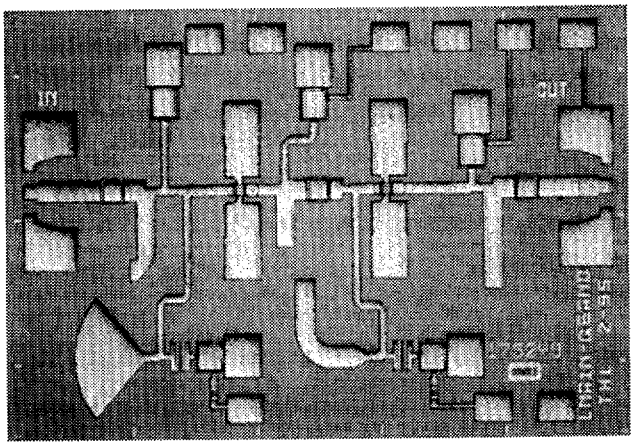

Figure 5. Layout of two-stage Q-band MMIC LNA

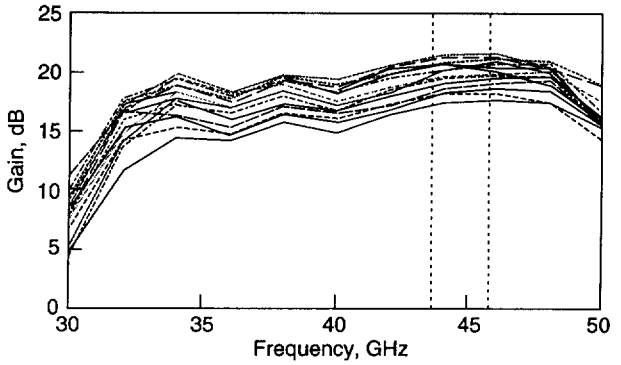

Figure 6a. Yield data for two-stage Q-band MMIC LNA

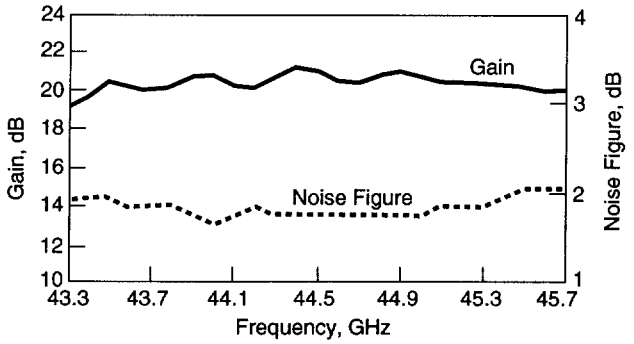

Figure 6b. Gain and noise figure for two-stage Q-band MMIC LNA

to 45.7 GHz (see Figure 6b). To our knowledge, this is the best reported average noise figure for a two-stage MMIC LNA in this frequency band. The chip size is 1.5 × 2.5 mm.

BALANCED TWO-STAGE Q-BAND LNA

This MMIC utilizes four 50 × 0.1 μm HEMTs (Figure 7). All stages are biased and matched for low noise (1V at 7.5 mA). Identical Lange couplers were placed at the input and output of the LNAs to achieve a good match when the devices are biased on or off. This is useful in a switch application. All four drains are connected and all four gates are connected thereby requiring only two external dc bias lines. This feature is a major advantage in module integration since the layout is greatly simplified and serves to keep the channel width narrow to prevent waveguide moding. Operated at 1V and 30 mA total, these balanced LNAs provide an average gain of 17 dB from 42 to 50 GHz with 61% yield (see Figure 8a). The average noise figure is 2.6 dB (see Figure 8b). When drain bias is switched off, the balanced LNA provides 45 dB of channel isolation. The chip size is 2.0 × 3.0 mm.

FOUR-STAGE V-BAND LNA

The first stage of this amplifier uses a 100 × 0.1 μm HEMT and is biased and matched for low noise (Figure 9). Choosing this device size simplifies the input matching network and improves the passband flatness. The

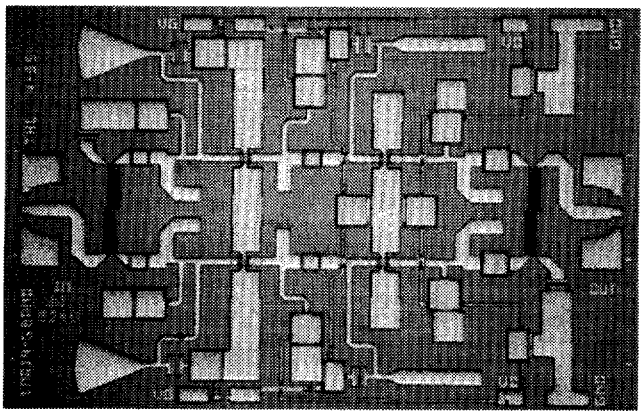

Figure 7. Layout of balanced two-stage Q-band MMIC LNA

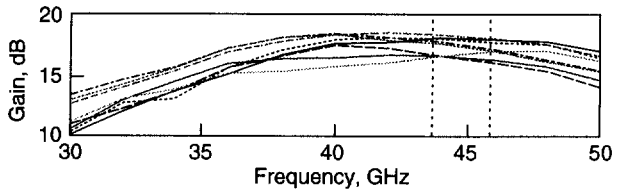

Figure 8a. Yield data for balanced two-stage Q-band MMIC LNA

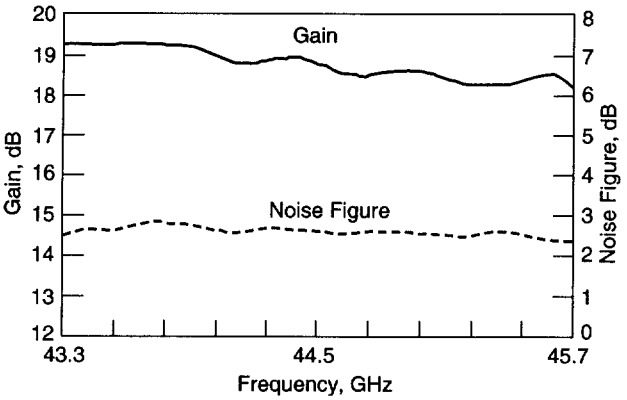

Figure 8b. Gain and noise figure for balanced Q-band MMIC LNA

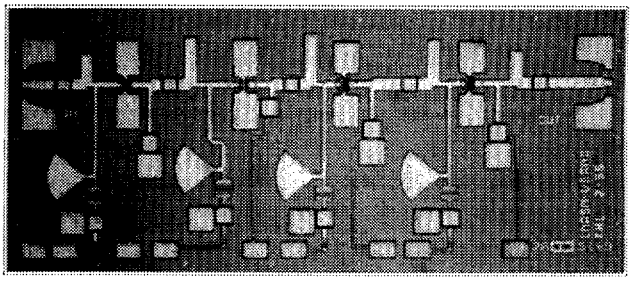

Figure 9. Layout of four-stage V-band MMIC LNA

second stage is a 50 × 0.1 μm device which is also biased and matched for low noise. Third and fourth stages have 150 × 0.1 μm devices that are biased and matched for high gain. These larger devices were used at the output to provide better than 5 dBm output power. Microstrip lines, open stubs and MIM capacitors were used for the input, interstage and output matching circuitry. Like the Q-band LNAs, quarter-wave length lines, microstrip radial stubs,

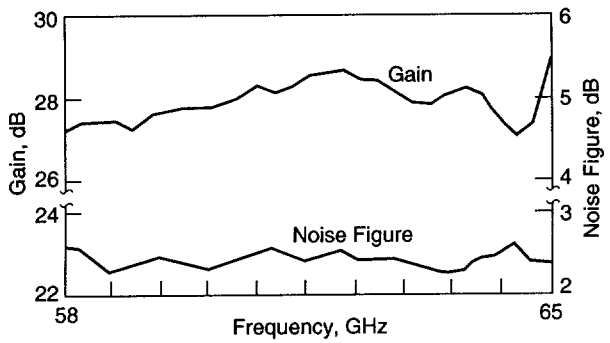

Figure 10. Gain and noise figure for four-stage V-band MMIC LNA

and epi resistors were used to stabilize the devices. Occupying an area of 1.5 × 3.5 mm and consuming 112 mW, this LNA achieved 28 dB of gain and 2.3 dB minimum noise figure from 58 to 65 GHz (see Figure 10).

THREE-STAGE V-BAND LNA

Designed around a 50 µm and two 150 × 0.1 µm devices, this 1.5 × 2.5 mm MMIC provides over 20 dB gain and 2.4 dB noise figure from 58 to 64 GHz (see Figures 11 and 12). The first stage is biased and matched for low-noise while the second and third stages are biased and matched for high gain. The dc consumption is 98 mW and the circuit provides 5 dBm output power.

TWO-STAGE V-BAND LNA

Designed to be an output amplifier that provides gain, power, and moderate noise figure, this MMIC contains two 150 × 0.1 µm devices that are both biased and matched for gain. Dissipating 90 mW of dc power, its measured gain is 13 dB minimum with a noise figure of 2.2 dB from 56 to 61 GHz (see Figures 13 and 14). The 150 µm output device was chosen to provide better than 5 dBm output power. The chip size is 1.5 × 2 mm.

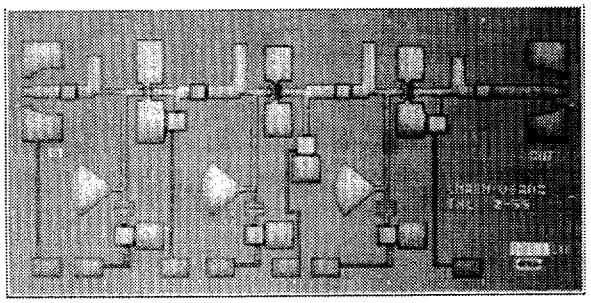

Figure 11. Layout for three-stage V-band MMIC LNA

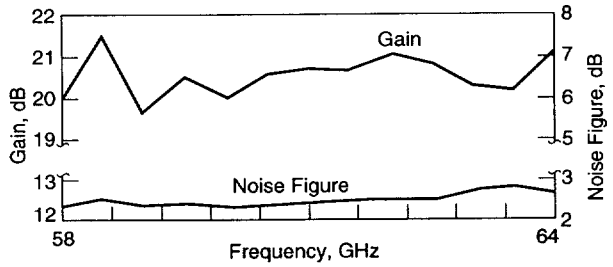

Figure 12. Gain and noise figure for three-stage V-band MMIC LNA

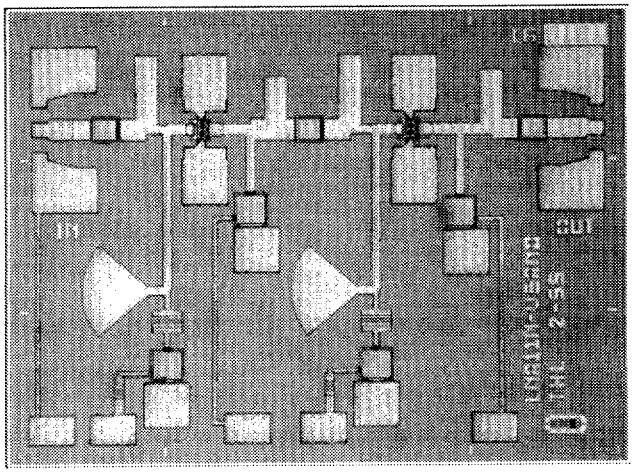

Figure 13. Layout of two-stage V-band MMIC LNA

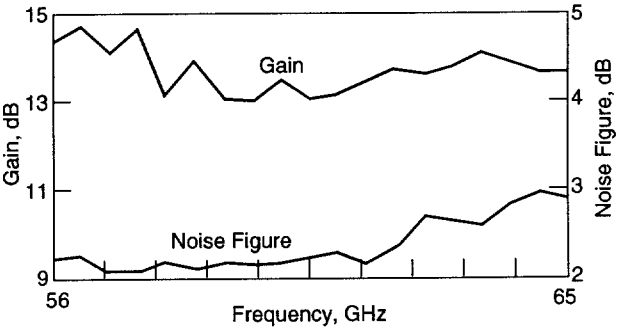

Figure 14. Gain and noise figure for two-stage V-band MMIC LNA

SUMMARY

Seven different MMIC LNAs were designed and fabricated. The test measurements reveal state-of-the-art performances with excellent yield and repeatability. The highlights are as follows: a three-stage Q-band LNA with 1.8 dB average noise figure from 43.3 to 45.7 GHz and over 50% yield for gain; a four-stage Q-band LNA with 56% yield for gain from 42 to 50 GHz; a two-stage balanced Q-band LNA with 17 dB of gain and a yield of over 61%; a four-stage V-band LNA with 2.3 dB minimum noise figure from 58 to 65 GHz and 28 dB of gain.

ACKNOWLEDGMENTS

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[2] L. Nguyen, et al; 1993 IEEE MTT-S Digest pp 345-7